High-Output, Single- and Dual-Diode, Millimeter-Wave Frequency Doublers

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Abstract — **A balanced, dual-diode varactor frequency doubler for 85–116 GHz is described and its performance compared to that of a single-diode device. The balanced doubler can provide a minimum of 18 mW between 85 and 116 GHz for 190-mW maximum safe input power, while the single-diode doubler using the same diode-type exhibits a minimum output power of 10 mW over the same frequency range for a maximum safe input power of 90 mW. An improved single-diode design using a higher breakdown voltage diode has achieved a minimum output power of 18 mW between 97 and 116 GHz for a maximum safe input power of 150 mW. These devices have been used in cascade with a frequency tripler to implement a 6× multiplier chain to 310–350 GHz with a minimum output power in this submillimeter band of 0.6 mW.**

I. Introduction

IN RECENT YEARS, frequency multipliers have become widely used to provide a reliable, low-cost source of local oscillator power in millimeter wavelength heterodyne receivers. Extending this technology to the submillimeter band without the use of costly klystron pump sources for doublers and triplers necessitates the development of high-order multiplier chains with adequate efficiency to provide useable power at frequencies above 300 GHz. A recent paper described the design of an efficient, quasi-optical frequency tripler for 260–350 GHz [1], which exhibited best conversion efficiency for a pump input level of about 30 mW. This paper describes frequency doublers with an output frequency range compatible with the quasi-optical tripler input band and with sufficient output power to pump the tripler at an efficient operating level. The design of a practical dual-diode doubler is outlined, and measured performance data are presented and compared to results obtained with two versions of an earlier single-diode 2× multiplier [2]. The performance of the complete 6× multiplier chain is described.

II. Diode Specifications

The Schottky-barrier varactor diodes used in the multipliers described in this paper were manufactured by R. Mattauch at the University of Virginia and are of two types. The first, designated Type 5M2, is fabricated on 1.5-μm-thick vapor-phase epitaxially grown GaAs material doped to 2.6×10^{16} cm^{-3}. The second, designated Type 6P2, is on similar material with thickness 1.1 μm and doping 1.6×10^{16} cm^{-3}. Both material samples exhibit relatively uniform doping down to an abrupt epi-substrate transition zone, approximately 100 Å thick. Such a structure results in a high dynamic cutoff frequency [4], high breakdown voltage varactor diode. Both diodes have a typical zero bias capacitance of 20 fF, a dc series resistance of 6–8 Ω, and the breakdown voltage is typically 14 or 18 V for the 5M2 or 6P2, respectively. Typical junction capacitance versus voltage responses are shown in Fig. 1 for the two diodes. From this figure it can be seen that the 5M2 diode approaches the behavior of an ideal abrupt junction varactor more closely than does the 6P2. Thus, although the 6P2 with its higher breakdown voltage should be capable of handling higher power levels, the 5M2 would be expected to give higher conversion efficiency in a given mount, because of its more nonlinear capacitance versus voltage response.

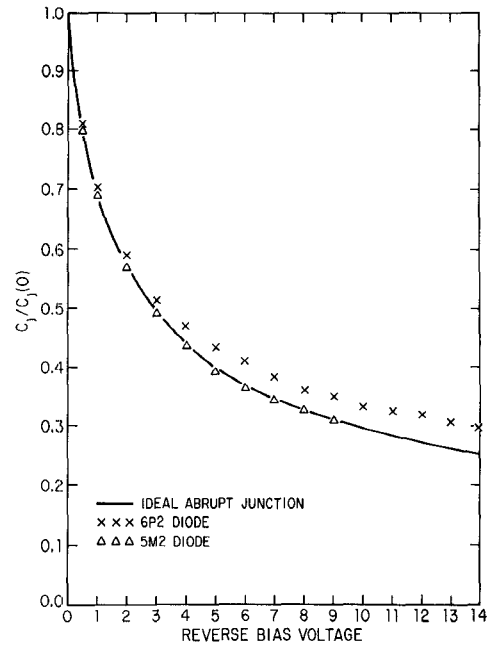

Fig. 1. Normalized junction capacitance versus reverse voltage for an ideal abrupt junction varactor (predicted using $C(V) = C(1 - V/\phi)^{-1/2}$) and for typical 5M2 and 6P2 diodes (measured).

III. Balanced, Two-Diode, Varactor Doubler

For a given diode, the output power of a single-diode varactor multiplier can be maximized by careful mount

Manuscript received August 8, 1984; revised January 30, 1985.

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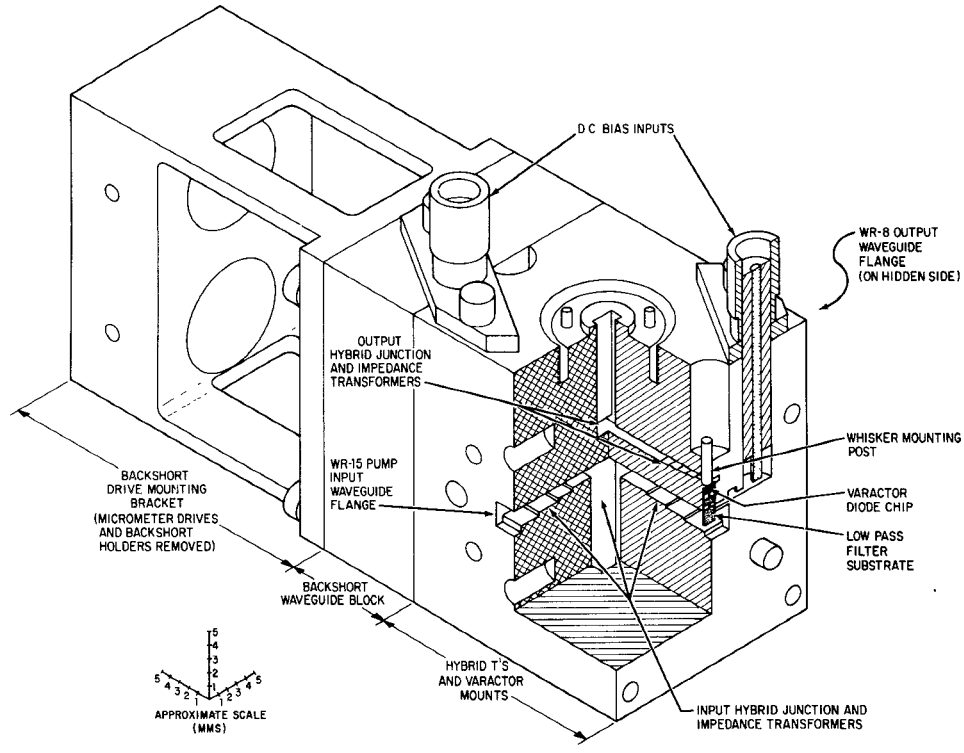


Fig. 2. An isometric drawing, approximately to scale, showing the main features of the balanced doubler design. Dimensions are in millimeters.

optimization [3]. To achieve a further significant increase in multiplier output power, a diode with a significantly greater breakdown voltage may be installed in the mount [3] or, alternatively, a new mount may be designed in which the input signal is split between two identical diodes and then the desired harmonic output component from each varactor recombined with the correct phase relationship. In the absence of losses, a dual-diode device of this type should double the maximum power level available with no degradation in efficiency. The balanced doubler described in this paper incorporates two identical varactor mounts coupled together, for the purpose of power combining or dividing, by waveguide 4-port T junctions ("magic T"'s). Fig. 2 shows a drawing which illustrates the concept.

The matched waveguide hybrid T's used in the mount at the input and output frequencies are, except for the waveguide transformer designs, geometrically scaled versions of one another. In order to achieve a wide impedance matched operating bandwidth, the waveguide height for the H-plane section is reduced to half the height of the E-plane arm. The H-plane arm is matched with a cylindrical post inside the junction, and the E-plane arm is matched with an asymmetric inductive iris. Multisection, quarter-wave step transformers are incorporated to couple the magic T's to the waveguides of the varactor mounts. The critical dimensions of the lower frequency waveguide junction, matching elements, and step transformer are shown in Fig. 4. The hybrid T's have theoretical center frequencies of 57 GHz and 105 GHz and are expected to exhibit VSWR's of less than 1.20 over about a 20-percent bandwidth.

The varactor mounts are similar in many respects to earlier NRAO designs [2],[5]. However, in the present device, both the input and output waveguides are normal to the plane of the stripline low-pass filter substrate. Pump power is coupled from the full height input guide, via the hybrid T and waveguide impedance transformers, to the full height (3.75×1.88 mm) pump waveguide of each varactor mount. Probe-type waveguide to stripline transitions, each tuned with a single contacting sliding short, then inject the pump signal into the stripline low-pass filters. The filters are high/low impedance transmission line realizations of a lumped-element, seven-section 0.1-dB ripple Chebycheff design, with a cutoff frequency of 65 GHz. The stripline configuration is a scaled version of a modified suspended substrate structure described recently by Archer [6], using a 0.127-mm-thick chrome/gold metallized, crystalline quartz dielectric substrate. The critical dimensions of the filter are shown in Fig. 3.

The varactor diodes are mounted on the low-pass filter substrate adjacent to the output waveguide. Each diode can be independently dc biassed via a transmission-line bias filter connected to the low-pass filter metallization. The outer shield of the bias line is a 0.25-mm-wide channel of square cross section milled into the surface of the block forming the mount. The center conductor is a length of 0.025-mm-diam gold wire bonded at one end to a low-impedance section of the low-pass filter and at the other end to a 100-fF metallized quartz dielectric bypass capacitor, which is epoxied in a recess located 1.25 mm from the connection to the low-pass filter. The line terminates on

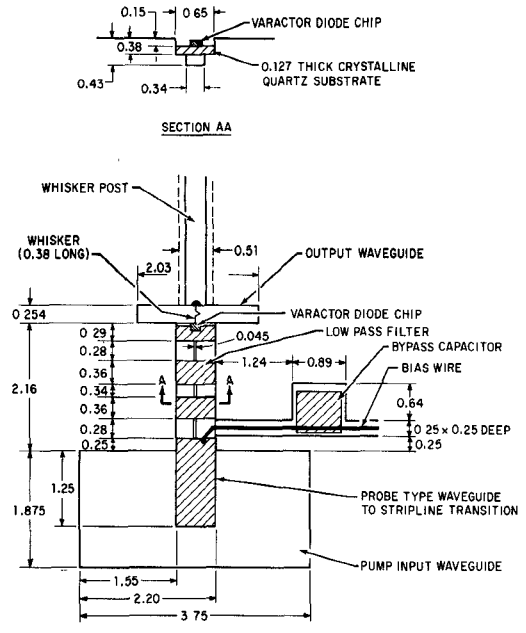


Fig. 3. A sketch showing details of the varactor mounting structure and stripline low-pass filter. Dimensions are in millimeters.

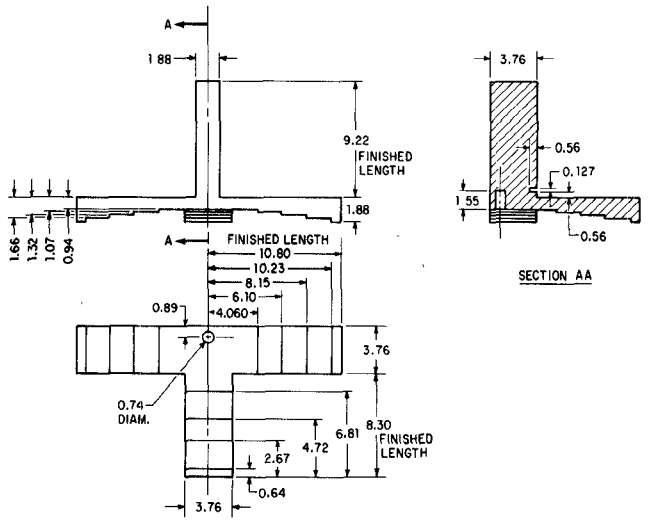


Fig. 4. A sketch showing the physical dimensions of the aluminum mandrel used to fabricate the lower frequency "magic T." The higher frequency "magic T" is a scaled version (×0.54) of the one illustrated and incorporating a different (1/4 to 1/2 height waveguide) impedance transformer. All dimensions are in millimeters.

the center pin of the SMA bias connector. The section of line between capacitor and filter approximates, at 120 GHz, a quarter-wave short-circuited stub of 140-Ω characteristic impedance.

The 2.03×0.25-mm output waveguide has height reduced to one quarter of the standard value. The reduced mount impedance at the second and higher harmonics is expected to improve the power-handling capability of the doubler by reducing the peak instantaneous voltage across the diode at a given input power. Each varactor chip is contacted by a 0.38-mm-long × 0.0127-mm-diam gold plated, phosphor–bronze whisker. The electrochemically pointed whisker is attached to a 0.51-mm-diam beryllium–copper post, which is an interference fit in a hole in the mounting block. The length of the contact whisker is chosen so that its inductance approximately series-resonates the average capacitance of the pumped varactor diode at the input frequency. Furthermore, this choice of whisker length theoretically provides, in conjunction with an adjustable contacting backshort, a convenient transformation between the diode impedance and the output waveguide impedance at the output frequency. Second harmonic power from each varactor mount is coupled to the output magic T via another pair of quarter-wave transformers, and the combined signal is then coupled to the output port.

The varactors used in the balanced doubler are type 5M2. Diodes were selected from a large batch in order to obtain two devices with well-matched dc characteristics. Measured parameters for the two devices were as follows: $C_j(0)-20.5$ and 21.1 fF, $R_s(\mathrm{dc})-8.5$ and 8.0 Ω, V_{br} (1 μA)−14.5 and 13.8 V.

The techniques used in the fabrication of the balanced doubler played an important role in the success of the design. Each hybrid T junction was separately electroformed on gold-plated aluminum mandrels in an acid copper bath. The electroforming was carried out in two stages, as shown in Fig. 5, in order to maintain precise perpendicularity of the arms of the T's and to ensure excellent symmetry of the junction. The matching elements were fixed into the copper waveguide walls by inserting slightly overlength, gold-plated posts and shims into holes cut in the mandrels prior to electroforming. The resultant accurately fabricated, internally gold-plated waveguide junctions were pressed into pre-milled slots in a pair of brass half blocks, which were then permanently fixed together to form the final doubler assembly. The waveguide flanges, stripline channels, whisker pin holes, and bias line structures were machined into the surfaces of this block to complete the device. The backshort waveguides were separately electroformed and then pressed into an additional pair of brass blocks which mate with the main assembly, as shown in Fig. 2.

IV. Performance Comparisons Between Dual- and Single-Diode Doublers

The performance of the balanced multiplier was measured at 1-GHz intervals for output frequencies between 85 and 120 GHz using an Anritsu thermocouple power meter. The output power response as a function of output frequency for a constant pump level of 190 mW (the maximum safe operating level—diode damage occurs above this input power) is shown in Fig. 7. Backshort tuning and dc bias were optimized for each of the two varactor mounts at each measurement frequency. Typically, the bias voltage for optimum performance was about 4.0 V with a forward current between 5 and 8 mA. More than 18-mW output was obtained at any frequency between 85 and 116 GHz,

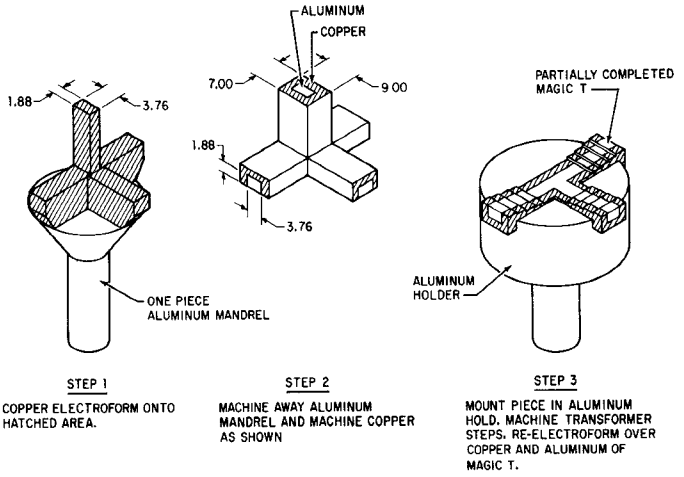
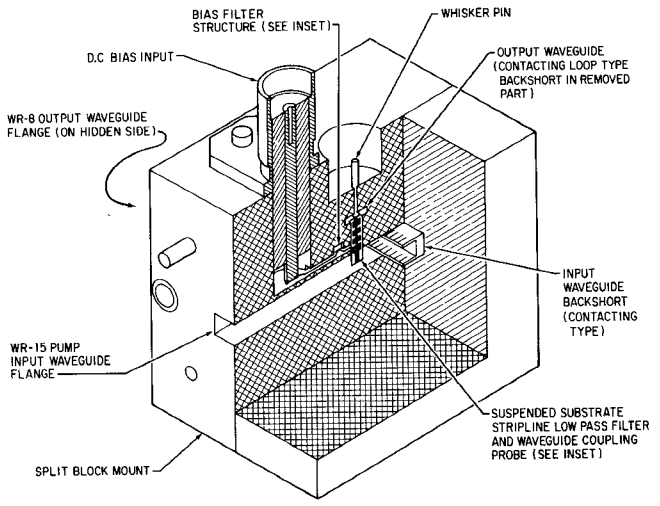


Fig. 5. The method of fabricating and holding the "magic T" mandrels during the electroforming process.



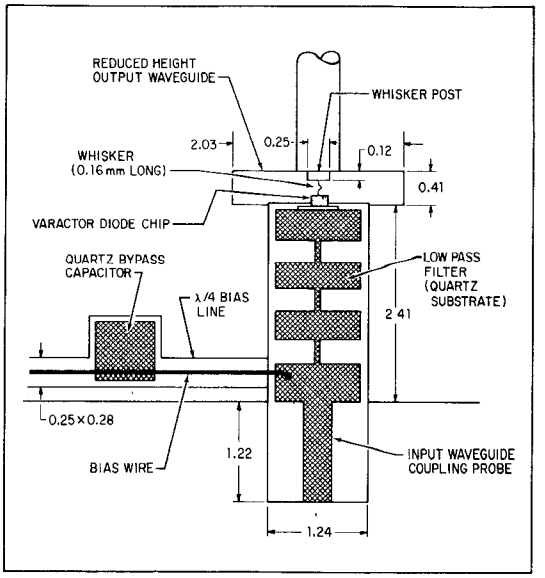


Fig. 6. An isometric drawing and sketch showing the main features of the single-diode doubler design and details of the varactor mounting and biasing structure. Dimensions are in millimeters.

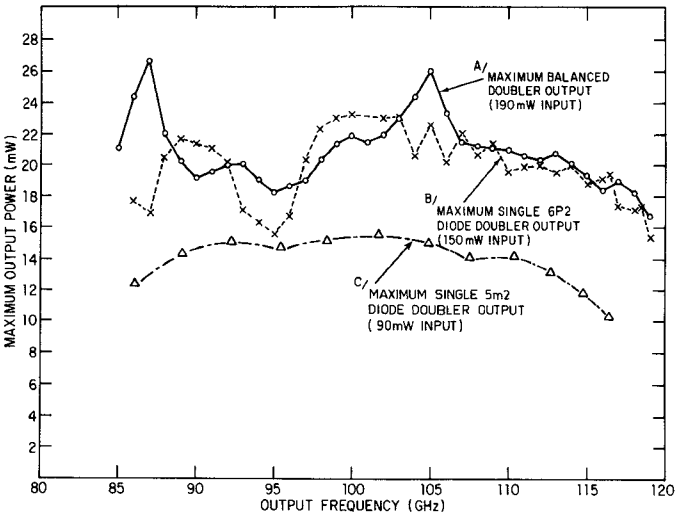


Fig. 7. Maximum output power versus output frequency for the balanced (curve *A*) and single-diode (curves *B* and *C*) doublers. DC bias and tuning were optimized at each measurement frequency.

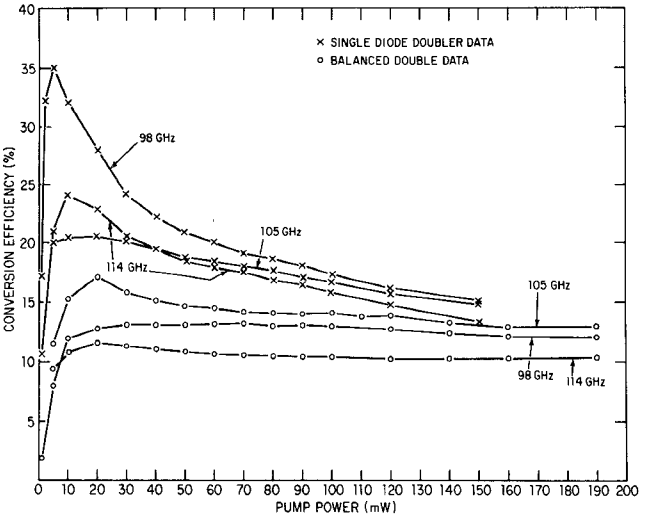


Fig. 8. Conversion efficiency versus pump power shown for the dual- and single-diode doublers at three representative frequencies. DC biasing and tuning were optimized at each measurement point.

corresponding to a minimum conversion efficiency at the 190 mW input level of 9.5 percent. Over most of this range, more than 20 mW was available, with a peak output power of 26.6 mW at 88 GHz, corresponding to an efficiency of 14 percent.

Higher conversion efficiencies may be attained with lower pump power. The maximum conversion efficiency typically occurs for pump powers of 80 mW. The relationship between pump power and efficiency is illustrated graphically in Fig. 8 for three different operating frequencies. Bias and tuning were adjusted for best performance at each pump level. With a pump power of 80 mW, a maximum efficiency of 16.5 percent is obtained at 104 GHz and the minimum efficiency between 85 and 116 GHz is 12 percent.

Fig. 7 also shows performance curves for two single-diode doublers. One of these multipliers was identical to a half-height waveguide mount described in an earlier paper [2] and incorporated a 5M2 diode similar to that used in

the balanced doubler. For a maximum safe input power of 90 mW, the minimum output power between 85–116 GHz is 10 mW, corresponding to a minimum conversion efficiency of 11.1 percent at this pump level. The maximum output of 15.75 mW occurs at 102 GHz, corresponding to a peak efficiency of 17.5 percent. Clearly, the balanced doubler *using the same diode type*, can provide significantly greater output power than the single-diode devices. However, the overall conversion efficiency is lower for the dual-diode doubler due to the higher ohmic losses in the more complicated waveguide structure. The second single-diode device, shown schematically in Fig. 6, incorporates a higher breakdown voltage varactor (type 6P2) and changes to the diode embedding circuit aimed at optimizing the high-power performance of the multiplier between 100 and 116 GHz. The whisker post diameter was reduced to 0.25 mm, the length of the post in the guide increased to about two-thirds of the guide height, and the whisker length shortened to 0.16 mm, resulting in significant improvements in performance at high-power levels in the desired band when compared to the results reported previously. For 150-mW input power (the maximum safe operating level), the minimum output power between 97 and 116 GHz is 18.5 mW, corresponding to a minimum conversion efficiency at the 150-mW pump level of 12 percent. The peak output power of 23.2 mW occurs at 100 GHz with a corresponding conversion efficiency of 15.3 percent. Typical dc bias conditions were about 6-V reverse bias with 1-mA to 3-mA forward current. As with the dual-diode doubler, the single-diode device exhibits improved conversion efficiency at lower pump levels, although for the latter the dependency is much more pronounced. The relationship is illustrated in Fig. 8. The maximum conversion efficiency achieved is 35 percent at 98 GHz for a pump power of 5 mW.

Clearly either the improved single-diode or the dual-diode doubler described above are capable of providing output power over the full 85–120-GHz range, which is significantly greater than that of previously reported multiplier sources. The balanced mount exhibits lower conversion efficiency than the new single varactor device due, as discussed above, to the higher ohmic losses in the more complex waveguide structure and possibly to the lower waveguide impedance mounting circuit. However, the lower efficiency can be traded off against its higher power handling capability and flatter efficiency versus pump power response when deciding whether to use the dual-diode or single-diode doubler in a given application. The single-diode doubler, being less complex, is easier to tune than the balanced device, and at low pump levels exhibits the highest conversion efficiency yet reported in the 85–120-GHz band.

V. 6× Multiplier Chain to the 310–350-GHz Band

The single- and dual-diode doublers reported above have been used in conjunction with a quasi-optical frequency tripler to implement a solid-state multiplier source in the 310–350-GHz range. The output of either doubler was directly connected to the tripler input via a short length of WR-8 waveguide; an isolator was not used between the multipliers. Fig. 9 shows the measured output power of the multiplier chain, with either doubler pumped at its maximum safe input level. The multiplier combination, for either doubler, was found to be surprisingly easy to tune for optimum performance at a given frequency, and the interaction between doubler and tripler adjustments was minimal.

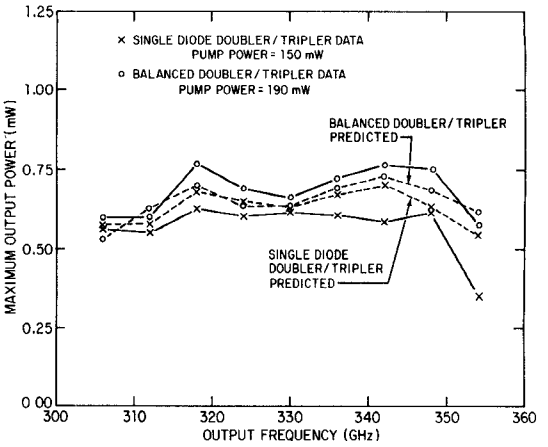


Fig. 9. Measured maximum output versus output frequency for the balanced doubler/tripler combination and for the single-diode doubler/tripler chain. DC bias and tuning for each mount were optimized at each measurement frequency. The graph also shows the predicted frequency response, based on measurements of the individual multipliers, after correcting for a loss of 0.15 dB in the interconnecting waveguide.

It can be seen that either multiplier chain provides a minimum output power of 0.6 mW between 310 and 350 GHz, with the balanced doubler/tripler combination giving approximately the output power predicted from the performance of the individual components. However, the output power of the single-diode doubler/tripler combination is less than would be expected from measurements of the performance of the separate devices. The explanation of this result is related to the way in which the initial single device measurements were performed. The output power of the doublers was measured using a very broad-band thermocouple power meter, which responds not only to power at the desired harmonic but also to higher harmonic components. Evaluations of the output spectrum of typical doublers and triplers have shown that the undesired harmonics are usually at least 15 dB below the desired output component [7]. Thus, measurements using the broad-band power meter should overestimate the multiplier efficiency by no more than 5 percent. The single-diode doubler described here appears to have significantly greater third-harmonic content in its output spectrum when operated at high pump power levels than the normal case. The ratio of third- to second-harmonic power output for the 120-mW pump level is estimated to be about 0.15. In contrast, the balanced doubler exhibits much lower third-harmonic conversion efficiency due to the poor perfor-

mance of the output hybrid T junction at frequencies outside its design band.

VI. Conclusion

This paper has shown that broadly tuneable, high output power frequency doublers can now be successfully fabricated for the 85–120-GHz band. Both single- and dual-diode devices have been built that are capable of generating power in excess of 20 mW in this band. These multipliers are ideally suited to use, in conjunction with an efficient frequency tripler, in the implementation of a 6× multiplier source with output frequency in the range 310–350 GHz. The multiplier chain described in this paper gives output power in excess of 0.6 mW in this submillimeter band. This is an adequate power level for local-oscillator applications in submillimeter, cooled Schottky-diode mixer receivers using low-loss quasi-optical LO injection schemes. If used in conjunction with a Gunn or IMPATT solid-state pump source, the multiplier chain enables the realization of the first useful, all solid-state, 310–350-GHz LO signal source.

Acknowledgment

The authors wish to thank G. A. Taylor for his excellent work in the fabrication of the components described in this paper. Thanks also go to N. Horner, Jr., who installed the diodes and chokes in the multiplier blocks. Prof. R. Mattauch of the University of Virginia supplied the varactor diodes for this project.

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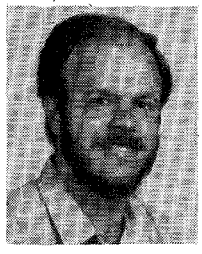

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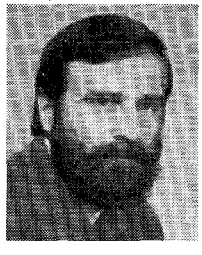

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